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EXAMINER	
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ART UNIT	PAPER NUMBER
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ip.department.us@nxp.com

Office Action Summary	Application No.	Applicant(s)	
	10/525,597	BENVENUTO ET AL.	
	Examiner	Art Unit	
	MICHAEL R. NEFF	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 October 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12,17-28 and 33* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12, 17-28, 33* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments filed 10/27/2008 have been fully considered but they are not persuasive. The examiner thoroughly reviewed the applicant's arguments but firmly believes that the cited reference reasonably and properly meets the claimed limitation as rejected.

Applicant's argument: "The claim rejections should be reversed because the primary '702 reference (upon which all rejections rely) is fundamentally unrelated to the claimed invention, which is directed to single carrier modulation. As described in its "Field of the Invention" and consistent with its entire specification, the '702 reference is directed specifically to "multipath propagation during the RF transmission of a digital signal." The '702 reference's approach involves using a multiplexer (e.g., 12 in FIG. 4) to process and weight a multipath digital signal. As is consistent with the discussion of these disparate approaches at paragraph 0008 of the instant application, this multipath approach is inconsistent with and fails to correspond to the claimed single carrier modulation, and cannot operate to correspond to the same. This is also consistent with various technical treatises and other sources, as readily available in the art."

Examiner's response: The examiner respectfully disagrees with the applicant that the '702 reference is applied improperly. Both the current application and the '702 reference feature disclosures directed towards frequency domain decision feedback devices. Per the disclosure of '702 at Col. 1 lines 5-11 the

multipath embodiment being argued is a given as an "example". The Examiner maintains the arts are directed towards fundamentally equivalent areas and that the application of the '702 reference is proper. Therefore the grounds of rejection are maintained and the prior art maintained as reasonable and proper in the rejection of the current application by the Examiner.

Applicant's argument: "Regarding the independent claims (1 and 18, respectively directed to device and method limitations with similar impart), the cited '702 reference thus cannot correspond to the claimed single carrier modulation and related "equalization means" that processes single carrier signals. The cited multiplexer 12 (i. e., for processing/multiplexing a multi carrier signal) thus does not correspond to the claimed single-carrier "equalization means," and the '702 reference therefore does not disclose claim limitations including "a feed forward equalization means for performing a feed forward equalization by multiplying each of the components of said second vector of signals with equalization parameters."

Examiner's response: Applicant's arguments fail to comply with 37 CFR 1.111(b) because they amount to a general allegation that the claims define a patentable invention without specifically pointing out how the language of the claims patentably distinguishes them from the references.

Regarding the first argument the examiner respectfully disagrees, again citing that the '702 reference is proper in application to the current application. Thus through the original citation the means of equalization are maintained as properly

cited in the prior art wherein the claimed limitations are fully encompassed. Following with the final argument above that the feed forward equalization means are not properly disclosed the examiner again disagrees, again citing the initially cited FF element along with the remaining previously cited disclosure as fully encompassing this claim limitation.

Applicant's argument: "In addition, the cited "multiplexer 12" multiplies the multipath carrier blocks by "2M weighting coefficients," which do not correspond to the claimed equalization means and its multiplication of a single carrier signal by equalization parameters. For example, as consistent with the discussion at paragraph 0036 of the instant invention and with various claim limitations (see, e.g., claim 3), equalization parameters used for single carrier modulation can be "generated by taking into account a fast Fourier transformation estimation of a channel impulse response of the (single carrier) signal processed." The cited weighting coefficients in the '702 reference do not contemplate such equalization in weighting the symbols, instead involving multipath signal processing and using "variants of the (multipath) transmission channel" as discussed at column 7:56-58. Moreover, calculation of the '702 reference's weighting coefficients "requires a large number of operations" due to this multipath approach, and thus "is done most of the time on a deferred time basis by a digital signal processor (DSP) type of computation device" as discussed at column 7:60-63."

Examiner's response: In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features

upon which applicant relies (i.e., large number of operations argument presented) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Initially the applicant is arguing subject matter which is not in the claim language in an effort to distinguish the '702 prior art from the current application. Following the previously cited FFT element of 11 is used in the FF process. Further, looking at Col. 7 lines 56-63 of the cited prior art the relationship between the weights and other system elements is established in the current prior art, fully encompassing the claimed limitations of the current application as provided.

Applicant's argument: "In addition to the above-discussed lack of correspondence as provided in the '702 reference, Applicant submits that the secondary '078 reference fails to disclose all of the limitations as asserted. For instance, the alleged "adding means" 22 is in fact a subtracter circuit that subtracts estimated distortion samples from input symbols (see, e.g., column 3:59-4:2), and thus fails to teach or suggest limitations directed to "adding the output signal of said feedback filter means to the output signal of said first section.""

Examiner's response: The Examiner respectfully disagrees with the applicant's assertion that the cited areas are improper in rejecting the current application. The essence of an add or subtract element are based on mathematical

properties. It is therefore entirely possible for adders to subtract (A + -B) or for a subtraction device to add (A - -B). Based on these common and well known mathematical properties and the well known abilities of the manipulation of data in a communication system, the examiner maintains that the cited area is in fact proper in the rejection of the limitations in discussion.

Applicant's argument: "Specifically regarding the rejection of claims 2 and 19, the Office Action's citation to the '702 reference's approach to minimize intersymbol interference does not disclose, teach or suggest minimizing the signal-to-noise ratio as claimed. The Office Action appears to have equated intersymbol interference with noise, without providing any explanation for the same. Applicant has reviewed the cited references and, as consistent with technical resources, intersymbol interference and noise may be related but are not one and the same."

Examiner's response: The disclosure of Col. 3 lines 5-9 shows a clear explanation for the application of the cited disclosure of the prior art towards the limitations of the claims as currently provided. The examiner respectfully disagrees with the applicant's position, and maintains the provided rejection.

Applicant's argument: "Specifically regarding the rejection of claims 3 and 20, the Office Action's citation to portions o the '078 reference, which simply mention channel impulse, do not disclose, teach or suggest the claimed equalization means and its functions relating to using a "fast Fourier transformation estimation of a channel impulse response" to generate equalization parameters. The '078

reference's discussion of impulse do not mention and do not appear to bear any relationship to fast Fourier transformation estimation of such an impulse, and further do not discuss generating equalization parameters in accordance with the same. Moreover, the Office Action has failed to provide any motivation whatsoever for combining the cited teachings as asserted in rejecting claims 3 and 20 (see pages 4 and 5 of the Office Action, which address claims 3 and 20)."

Examiner's response: The Examiner respectfully disagrees with the applicant's stated position. Again citing Col. 7 lines 56-63 as further explanation towards the originally cited material, the Examiner maintains that the cited references properly meet the claimed limitations. Further the applicant argues that no motivation has been provided, while the Examiner has provided motivation for the combination in claim 1 on which claim 3 depends. Respectfully the examiner maintains the position and ground of rejection of the above mentioned claims as currently presented.

Applicant's argument: "Regarding the rejection of claims 4 and 21, the indicated "M/PL element" acts after the forward filter FF and thus does not disclose converting a sequence of incoming signals for a first vector as claimed (e.g., the first vector is provided for fast Fourier transform as in claim 1). Correspondingly, the rejections of claims 4 and 21 as well as claims 5-8 and 22-25, which depend from either claim 4 or 21, are improper."

Examiner's response: Applicant's arguments fail to comply with 37 CFR 1.111(b) because they amount to a general allegation that the claims define

a patentable invention without specifically pointing out how the language of the claims patentably distinguishes them from the references. The Examiner respectfully disagrees with the applicants position and as no concise argument is present as to the differences between the prior art and the current application, the examiner maintains that the cited areas are reasonable and proper in the rejection of the cited claims and all further examiner claims alleged by the applicant to be improper.

Applicant's argument: "Regarding the Section 103 rejection of claims 11 and 28, the Office Action has not asserted that either reference teaches providing an output signal built by consecutive blocks, where each block includes "a predetermined number (M) of samples from" an output signal. In addition, while the secondary '574 reference describes a pseudo-random noise generator, it does not disclose including a pseudo noise sequence with blocks of an output signal as claimed. This is consistent with Applicant's previous response, which has not been addressed in the instant Office Action."

Examiner's response: Applicant's arguments fail to comply with 37 CFR 1.111(b) because they amount to a general allegation that the claims define a patentable invention without specifically pointing out how the language of the claims patentably distinguishes them from the references.

Regarding the initial argument the examiner maintains the original cited grounds of rejection further including Col. 6 lines 36-45 fully encompass the claimed limitation. Further regarding the argument towards the '574 reference, the

examiner disagrees with the applicant's position and again points to the previously provided grounds of rejection which reasonably and clearly point out the claimed limitation, as the applicant appears to be arguing a key word rather than the scope of the cited area of disclosure. Respectfully the examiner disagrees with the applicant's assertions, and has maintained the grounds of rejection as previously provided.

Applicant's argument: "In addition to the above, Applicant believes that there is no motivation for modifying the primary '702 reference as asserted to arrive at a single carrier approach because the reference is directed specifically to a multipath approach, and uses processing devices (multiplexer 12) and characteristics for multipath processing that are wholly unrelated to the claimed invention. Moreover, the secondary '078 reference appears to be directed to "a noisy, narrow band channel such as a telephone subscriber loop" (see the Technical Field), whereas the primary '702 reference is directed to "multipath propagation of a digital signal." In this context, Applicant believes that the alleged motivation is misplaced."

Examiner's response: The examiner respectfully disagrees with the applicants assertion that the prior arts are improper to combine as the '702 and '078 prior arts as cited are both in relation to decision feedback equalizers, allowing for one of ordinary skill in the art to draw connections between their disclosed designs. As the combination is viewed as proper by the examiner all connected rejections have been maintained.

Claim Rejections - 35 USC § 103

2. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

3. Claims 1-10, 18-27 and 33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Berberidis et al. (herein after Berberidis) (US Patent 6,052,702, see IDS) in view of Crespo (US Patent 5,020,078).

Re Claims 1 and 18, Berberidis discloses a frequency-domain decision feedback equalizer device for single carrier modulation, preferably for use in a broadband communication system, including a first section comprising: a fast Fourier transforming means (11) for performing a fast Fourier transformation on a first vector of signals (M, output from 10) inputted into said first section, and outputting a second vector of signals (2M), a feed forward equalization means for performing a feed forward equalization by multiplying each of the components of said second vector of signals with equalization parameters (12 and the associated inputs to element 12), and outputting a third vector of signals (output from element 12), and an inverse fast Fourier transforming means (13) for performing an inverse fast Fourier transformation on said third vector of signals, and outputting a fourth vector of signals (M, output from 13); while Berberidis discloses a second section comprising a feedback equalizer structure, the disclosure fails to explicitly disclose the feedback equalizer design wherein a second section comprising: a feedback filter means for performing a linear filtering of a signal derived from an output signal of said second section, an adding means for adding the output signal of said feedback filter means to the output signal of said first section, and a detector

means for receiving the output signal of said adding means and generating said output signal of said second section by extracting samples from the output signal of said adding means.

This design is however disclosed by Crespo. Crespo discloses a feedback filter means for performing a linear filtering of a signal derived from an output signal of said second section (33), an adding means for adding the output signal of said feedback filter means to the output signal of said first section (22), and a detector means for receiving the output signal of said adding means and generating said output signal of said second section by extracting samples from the output signal of said adding means (23; Col. 3 line 35-Col. 4 line 2).

Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the feed back equalizer design as disclosed by Crespo to modify the feedback equalizer design of Berberidis in order to gain the benefit of a dynamic and self corrective means of producing correct estimated symbols from the detector output directly.

Re Claims 2 and 19, the combined disclosure of Berberidis and Crespo as a whole disclose the device according to claims 1 and 18, Berberidis further discloses wherein said feed forward equalization means is provided for generating equalization parameters adapted for minimizing the signal-to-noise ratio of the signal processed in the frequency-domain decision feedback equalizer device, preferably in the output signal of said first section (FF, Col. 2 line 66-Col. 3 line 4; Col. 7 lines 42-55).

Re Claims 3 and 20, the combined disclosure of Berberidis and Crespo as a whole disclose the device according to claims 1 and 18, while Berberidis discloses the feed forward equalization branch comprising Fourier functionality (FF), wherein said feed forward equalization means is provided for generating equalization parameters by taking into account a fast Fourier transformation estimation of a signal (Col. 5 lines 64-Col. 6 line 8; FF block and inclusive FFT and multiplier components); Crespo further discloses wherein the signal is the channel impulse response of the signal processed in the frequency-domain decision feedback equalizer device, preferably in the output signal of said first section (Col. 3 line 34-Col. 4 line 2).

Re Claims 4 and 21, the combined disclosure of Berberidis and Crespo as a whole disclose the device according to claims 1 and 18; Berberidis further discloses wherein said first section further comprises: a serial to parallel converting means for converting a sequence of signals inputted into said first section to said first vector of signals (10, performs serial to parallel conversion of inputted signal [pre first section S/P manipulation]), and a parallel to serial converting means for converting said fourth vector of signals to a sequence of output signals of said first section (the M/PL element provides the ability to convert from parallel to serial; Col. 5 line 59-Col. 6 line 49 [post first section P/S conversion]).

Re Claims 5 and 22, the combined disclosure of Berberidis and Crespo as a whole disclose the device according to claims 4 and 21; Berberidis further discloses wherein said serial to parallel converting means is adapted to receive scalar signals (1, 10, x(n); Col.1 lines 31-44; Col. 2 lines 38-65; Col. 5 line 59-Col. 6 line 8).

Re Claims 6 and 23, the combined disclosure of Berberidis and Crespo as a whole disclose the device according to claims 4 and 21; Berberidis further discloses wherein said signal to parallel converting means is provided to generate said first vector of signals including blocks of a predetermined number (P) of consecutive samples of the signals inputted into said first section (Col. 5 lines 60-67).

Re Claims 7 and 24, the combined disclosure of Berberidis and Crespo as a whole disclose the device according to claims 4 and 21; Berberidis further discloses wherein said parallel to serial converting means and said feedback filter means are provided to output scalar signals (M/PL, y(n); Col. 2 lines 38-65, Col. 6 line 35-Col. 7 line 37).

Re Claims 8 and 25, the combined disclosure of Berberidis and Crespo as a whole disclose the device according to claims 6 and 23; Berberidis further discloses wherein said parallel to serial converting means is provided to output a scalar signal (Y) which is constituted by consecutive blocks of a predetermined number (M) of samples, each block being built with the predetermined number (M) of samples of each block of

said fourth vector of signals (Abstract; Col. 5 line 59-Col. 6 line 63; further Col. 6 line 64-Col. 7 line 6).

Re Claims 9 and 26, the combined disclosure of Berberidis and Crespo as a whole disclose the device according to claims 1 and 18; Berberidis further discloses wherein said detector means is adapted to receive and output discrete time signals (Col. 1 lines 5-67, Col. 6 line 64-Col. 7 line 37; Claim 3).

Re Claims 10 and 27, the combined disclosure of Berberidis and Crespo as a whole disclose the device according to claims 1 and 18; Berberidis further discloses wherein said detector means is provided to generate said output signal (DO, y(n); Col. 5 line 59-Col. 6 line 63).

Re Claim 33, Berberidis discloses a frequency-domain decision feedback equalizer device for single carrier modulation, the device comprising: a first section including a fast Fourier transformer (M) to perform a fast Fourier transformation on a first vector of single carrier signals (M, output from 10) inputted into said first section, and to output the transformed signals as a second vector of signals (2M),

a feed forward equalizer to perform a feed forward equalization by generating equalization parameters (12 and associated inputs to 12) using a fast Fourier transformation estimation of a channel impulse response of an output single carrier

signal of said first section(Col. 3 line 34-Col. 4 line 2; Col. 7 lines 56-63; Col. 5 lines 64-Col. 6 line 8; FF block and inclusive FFT and multiplier components),

multiplying each of the components of said second vector of signals with the generated equalization parameters to reduce the signal-noise ratio of the signals (FF; Col. 2 line 66-Col. 3 line 4; Col. 3 lines 5-9; Col. 7 lines 42-55),

and outputting the multiplied signals as a third vector of signals (output of 12), and

an inverse fast Fourier transformer to perform an inverse fast Fourier transformation on said third vector of signals (M, output of 13), while Berberidis discloses a second section comprising a feedback equalizer structure, the disclosure fails to explicitly disclose the feedback equalizer design wherein a second section comprising: a feedback filter means for performing a linear filtering of a signal derived from an output signal of said second section, an adding means for adding the output signal of said feedback filter means to the output signal of said first section, and a detector means for receiving the output signal of said adding means and generating said output signal of said second section by extracting samples from the output signal of said adding means.

This design is however disclosed by Crespo. Crespo discloses a feedback filter means for performing a linear filtering of a signal derived from an output signal of said second section (33), an adding means for adding the output signal of said feedback filter means to the output signal of said first section (22), and a detector means for receiving the output signal of said adding means and generating said output signal of

said second section by extracting samples from the output signal of said adding means (23; Col. 3 line 35-Col. 4 line 2).

Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the feed back equalizer design as disclosed by Crespo to modify the feedback equalizer design of Berberidis in order to gain the benefit of a dynamic and self corrective means of producing correct estimated symbols from the detector output directly.

4. Claims 11 and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Berberidis and Crespo as applied to claim 1 and 18 above, and further in view of Johnson et al. (herein after Johnson) (US Patent 5,808,574).

Re Claims 11 and 28, the combined disclosure of Berberidis and Crespo as a whole disclose the device according to claims 1 and 18; Berberidis further discloses wherein said second section further comprises a feedback input generator means for receiving said output signal of said second section and providing an output signal which is built by consecutive blocks, each block comprising a predetermined number (M) of samples from said output signal of said section, to said feedback filter means (Abstract; Col. 5 line 59-Col. 6 line 63; further Col. 6 line 64-Col. 7 line 6); however Berberidis fails to explicitly disclose wherein each block is also including a pseudo noise sequence.

This design is however disclosed by Johnson. Johnson discloses a feedback system within a communication system wherein the signals within the feedback loop are adjusted to include a pseudo noise sequence (Col. 45 lines 29-43).

Therefore it would have been obvious to one of ordinary skill in the art a the time the invention was made to modify the feedback equalizer disclosure of Berberidis to insert pseudo noise into the feedback signal as disclosed by Johnson in order to gain the benefit of improving on system performance and symbol detection.

5. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Berberidis and Crespo as applied in claim 1 above, and further in view of Gay-Bellile et al. (herein after Gay) (US Publication 2002/0070796 A1).

Re Claim 12, the combined disclosure of Berberidis and Crespo as a whole disclose the device according to claim 1; Berberidis further discloses, wherein said receiver includes said first and second sections of the frequency-domain decision feedback equalizer device according to claim 1 (see rejection for claim 1 above); however the disclosure fails to explicitly disclose using a single carrier modulation within the equalizer.

However this system design is disclosed by Gay. Gay discloses a feedback equalizer device wherein single carrier modulation is used (Paragraphs0016, 20, 24-26).

Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the use of single carrier modulation within the feedback equalizer system as disclosed by Gay with the feedback equalizer disclosure of Berberidis in order to gain the benefit of having a system that can perform with lower power consumption than that of a system using multi-carrier modulation.

6. **Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Berberidis and Gay as applied in claim 1, and further in view of Thomas et al. (herein after Thomas) (US Publication 2004/0013084 A1).**

Re Claim 17, the combined disclosure of Berberidis and Crespo as a whole disclose the device according to claim 1; Berberidis further discloses a communication system including a transmitter for transmitting data, comprising a modulating means for organizing the data in blocks a receiver of a communication system, wherein said receiver includes a frequency-domain decision feedback equalizer device (see rejection of claim 1 above); however Berberidis fails to explicitly disclose wherein (1) the communication system is using a single carrier modulation, and although the use of a header on a data signal is well known to those of ordinary skill in the art, Berberidis does not explicitly disclose (2) wherein each block is separated by a sequence of a predetermined signal.

Regarding item (1) above, this system design is disclosed by Gay. Gay discloses a feedback equalizer device wherein single carrier modulation is used (Paragraphs0016, 20, 24-26).

Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the use of single carrier modulation within the feedback equalizer system as disclosed by Gay with the feedback equalizer disclosure of Berberidis in order to gain the benefit of having a system that can perform with lower power consumption than that of a system using multi-carrier modulation.

Regarding item (2) above, separating each data block by a sequence of a predetermined signal, or a signal header, is explicitly disclosed by Thomas (Fig. 1-5).

Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate separating the data symbol blocks by a predetermined header symbol as disclosed by Thomas with the feedback equalizer as disclosed by Berberidis in order to gain the benefit of improved symbol recognition and demodulating within the receiver end of the communication system.

Conclusion

7. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to MICHAEL R. NEFF whose telephone number is

(571)270-1848. The examiner can normally be reached on Monday - Friday 8:00am - 4:30pm EST ALT Fridays.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Shuwang Liu can be reached on (571)272-3036. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/MICHAEL R. NEFF/
Examiner, Art Unit 2611
/Shuwang Liu/
Supervisory Patent Examiner, Art Unit 2611